Carrying out the plan:

* Low level module : incre, addition, addcarry, addcomple, sub, decre
* Top level module : secondaluu
* Verilog code :

module secondaluu(

input [7:0] a,

input [7:0] b,

input cin1,

input [4:0] s,

output reg [7:0] Y,

output reg Carryout

);

wire [7:0]Y2,Y3,Y4,Y5,Y6,Y7;

wire Carry4,Carry5,Carry6,Carry7;

incre incre1(a,Y2,Carry4);

addition addition1(a,b,Y3,Carry5);

addcarry addcarry1(a,b,Y4,Carry6);

addcomple addcomple1(a,b,Y5,Carry7);

sub sub1(a,b,Y6);

decre decre1(a,Y7);

always@(a,b,cin1,s,Y2,Y3,Y4,Y5,Y6,Y7,Carry4,Carry5,Carry6,Carry7)

begin

if(cin1==1'b0&&s==5'b00000)

begin

Y=a;

Carryout=1'b0;

end

else if(cin1==1'b1&&s==5'b00000)

begin

Y=Y2;

Carryout=Carry4;

end

else if(cin1==1'b0&&s==5'b00001)

begin

Y=Y3;

Carryout=Carry5;

end

else if(cin1==1'b1&&s==5'b00001)

begin

Y=Y4;

Carryout=Carry6;

end

else if(cin1==1'b0&&s==5'b00010)

begin

Y=Y5;

Carryout=Carry7;

end

else if(cin1==1'b1&&s==5'b00010)

begin

Y=Y6;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b00011)

begin

Y=Y7;

Carryout=1'b0;

end

else if(cin1==1'b1&&s==5'b00011)

begin

Y=a;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b00100)

begin

Y=a&b;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b00101)

begin

Y=a|b;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b00110)

begin

Y=a^b;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b00111)

begin

Y=~a;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b01000)

begin

Y=a<<1;

Carryout=1'b0;

end

else if(cin1==1'b0&&s==5'b10000)

begin

Y=a>>1;

Carryout=1'b0;

end

else if (cin1==1'b0&&s==5'b11000)

begin

Y=8'b00000000;

Carryout=1'b0;

end

else

begin

Y=1'b0;

Carryout=1'b0;

end

end

endmodule

module incre(

input [7:0] a,

output [7:0] s,

output Carry8

);

wire [7:0]b=8'b00000000;

wire cin1=1'b1;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7;

fulladder fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladder fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladder fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladder fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladder fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladder fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladder fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladder fa\_7( a[7], b[7], Carry7, s[7], Carry8);

endmodule

module addition(

input [7:0] a,

input [7:0] b,

output [7:0] s,

output Carry8

);

wire cin1=1'b0;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7;

fulladderr fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladderr fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladderr fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladderr fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladderr fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladderr fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladderr fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladderr fa\_7( a[7], b[7], Carry7, s[7], Carry8);

Endmodule

module addcarry(

input [7:0] a,

input [7:0] b,

output [7:0] s,

output Carry8

);

wire cin1=1'b1;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7;

fulladd fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladd fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladd fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladd fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladd fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladd fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladd fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladd fa\_7( a[7], b[7], Carry7, s[7], Carry8);

Endmodule

module addcomple(

input [7:0] a,

input [7:0] d,

output [7:0] s,

output Carry8

);

wire cin1=1'b0;

wire [7:0]b;

assign b=~d;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7;

fulladde fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladde fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladde fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladde fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladde fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladde fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladde fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladde fa\_7( a[7], b[7], Carry7, s[7], Carry8);

Endmodule

module sub(

input [7:0] a,

input [7:0] d,

output reg [7:0]df

);

wire cin1=1'b1;

wire [7:0]b,m;

assign b=~d;

wire [7:0]s;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7,Carry9;

negone negone1(s,m,Carry9);

fulladder fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladder fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladder fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladder fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladder fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladder fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladder fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladder fa\_7( a[7], b[7], Carry7, s[7], Carry8);

always@(a,d,cin1,Carry8,m,s)

begin

case(Carry8)

0:df=m;

1:df=s;

endcase

end

endmodule

module decre(

input [7:0] a,

output reg [7:0] df

);

wire cin1=1'b1;

wire [7:0] d=8'b00000001;

wire [7:0]b,m;

assign b=~d;

wire [7:0]s;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7,Carry9;

negone negone1(s,m,Carry9);

fulladder fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladder fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladder fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladder fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladder fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladder fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladder fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladder fa\_7( a[7], b[7], Carry7, s[7], Carry8);

always@(a,d,cin1,Carry8,m,s)

begin

case(Carry8)

0:df=m;

1:df=s;

endcase

end

endmodule

module negone(

input [7:0] n,

output [7:0] s,

output Carry8

);

wire [7:0]b=8'b00000000;

wire [7:0]a;

assign a=~n;

wire cin1=1'b1;

wire Carry1,Carry2,Carry3,Carry4,Carry5,Carry6,Carry7;

fulladder fa\_0( a[0], b[0], cin1, s[0], Carry1);

fulladder fa\_1( a[1], b[1], Carry1, s[1], Carry2);

fulladder fa\_2( a[2], b[2], Carry2, s[2], Carry3);

fulladder fa\_3( a[3], b[3], Carry3, s[3], Carry4);

fulladder fa\_4( a[4], b[4], Carry4, s[4], Carry5);

fulladder fa\_5( a[5], b[5], Carry5, s[5], Carry6);

fulladder fa\_6( a[6], b[6], Carry6, s[6], Carry7);

fulladder fa\_7( a[7], b[7], Carry7, s[7], Carry8);

Endmodule

module fulladder(

input wire a,

input wire b,

input wire cin,

output Sum,

output Carry

);

reg T1,T2;

assign Carry=(a&b)|(b&cin)|(a&cin);//Data flow modelling

always@(a or b or cin) //Behavioural Modelling

begin

T1=a^b;

T2=cin;

end

xor(Sum,T1,T2);// Structural modelling

endmodule

RTL Schematic :



Test Bench:

module dd\_tb;

// Inputs

reg [7:0] a;

reg [7:0] b;

reg cin1;

reg [4:0] s;

// Outputs

wire [7:0] Y;

wire Carryout;

// Instantiate the Unit Under Test (UUT)

secondaluu uut (

.a(a),

.b(b),

.cin1(cin1),

.s(s),

.Y(Y),

.Carryout(Carryout)

);

initial begin

// Initialize Inputs

a = 0;

b = 0;

cin1 = 0;

s = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

a=8'b10011010;

b=8'b11111111;

cin1=1'b1;

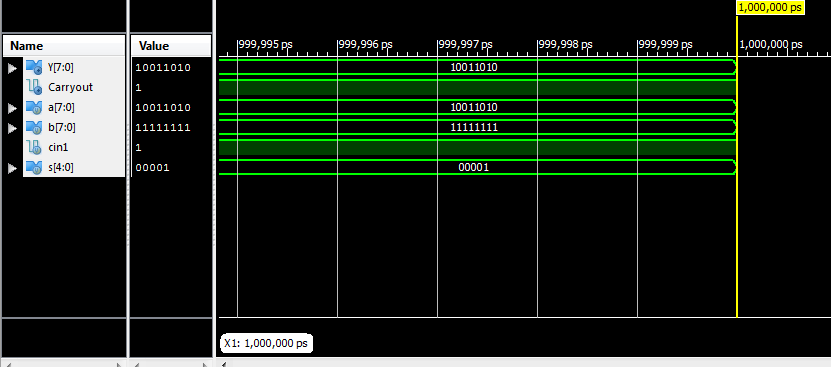
s=5'b00001;

#100;

end

endmodule

Output:



**Synthesis report:**

Design Statistics

# IOs : 31

Cell Usage :

# BELS : 196

# GND : 1

# LUT2 : 10

# LUT3 : 48

# LUT4 : 126

# MUXF5 : 10

# VCC : 1

# IO Buffers : 31

# IBUF : 22

# OBUF : 9

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Device utilization summary:

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Selected Device : 3s200pq208-5

Number of Slices: 105 out of 1920 5%

Number of 4 input LUTs: 184 out of 3840 4%

Number of IOs: 31

Number of bonded IOBs: 31 out of 141 21%

Timing Summary:

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Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 19.985ns

Timing Detail:

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All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 2018 / 9

-------------------------------------------------------------------------

Delay: 19.985ns (Levels of Logic = 12)

Source: a<1> (PAD)

Destination: Carryout (PAD)

Data Path: a<1> to Carryout

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 21 0.715 1.458 a\_1\_IBUF (a\_1\_IBUF)

LUT4:I1->O 2 0.479 1.040 addition1/fa\_1/Carry1 (addition1/Carry2)

LUT3:I0->O 2 0.479 1.040 addition1/fa\_2/Carry1 (addition1/Carry3)

LUT3:I0->O 2 0.479 1.040 addition1/fa\_3/Carry1 (addition1/Carry4)

LUT3:I0->O 2 0.479 1.040 addition1/fa\_4/Carry1 (addition1/Carry5)

LUT3:I0->O 2 0.479 1.040 addition1/fa\_5/Carry1 (addition1/Carry6)

LUT3:I0->O 2 0.479 0.804 addition1/fa\_6/Carry1 (addition1/Carry7)

LUT4:I2->O 1 0.479 0.000 Carryout65\_SW02 (Carryout65\_SW01)

MUXF5:I0->O 1 0.314 0.851 Carryout65\_SW0\_f5 (N99)

LUT4:I1->O 1 0.479 0.740 Carryout65 (Carryout65)

LUT3:I2->O 1 0.479 0.681 Carryout77 (Carryout\_OBUF)

OBUF:I->O 4.909 Carryout\_OBUF (Carryout)

----------------------------------------

Total 19.985ns (10.249ns logic, 9.736ns route)

(51.3% logic, 48.7% route)